Surface Reactions in Microelectronics Process Technology

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Abstract

Current integrated circuit (IC) manufacturing consists of more than 800 process steps, nearly all of which involve reactions at surfaces that significantly impact device yield and performance. From initial surface preparation through film deposition, patterning, etching, residue removal, and metallization, an understanding of surface reactions and interactions is critical to the successful continuous scaling, yield, and reliability of electronic devices. In this review, some of the most important surface reactions that drive the development of microelectronic device fabrication are described. The reactions discussed do not constitute comprehensive coverage of this topic in IC manufacture but have been selected to demonstrate the importance of surface/interface reactions and interactions in the development of new materials, processing sequences, and process integration challenges. Specifically, the review focuses on surface reactions related to surface cleaning/preparation, semiconductor film growth, dielectric film growth, metallization, and etching (dry and wet).

INTRODUCTION

Discovery of the first (Ge-based) transistor in 1947, followed by production of the first silicon transistor by Texas Instruments in 1954 (1) and the first Metal-Oxide-Semiconductor (MOS) transistor fabricated at Bell Labs in 1960 (2) initiated the microelectronics revolution. In the early 1960s Gordon Moore delivered his prophetic paper and defined the term integrated electronics (3). He projected that the packing density of electronic devices would grow exponentially, doubling approximately every year. In fact, during the past 50 years, the number of transistors per chip has doubled essentially every 18 months; semiconductor devices and integrated circuits (ICs) have thus become global enterprises. Consumer, communication, and computer products will continue to be the leading sectors driving the largest growth of the electronics industry. In 2014, the total industry is expected to top $1.4 trillion in annual assembly value (4).

Current IC manufacture consists of more than 800 process steps, nearly all of which involve surfaces that significantly impact device yield and performance. From initial surface preparation through film deposition, patterning, etching, residue removal, and metallization, an understanding of surface reactions and interactions is critical to the successful continuous scaling, yield, and reliability of electronic devices.

Film thicknesses and pattern sizes in devices and ICs have decreased continuously and are rapidly approaching the molecular and atomic scale. Therefore, the physical, chemical, and electrical properties of surfaces and interfaces, which establish device/IC properties, must be controlled and exploited at the nanoscale to allow continued advances in this technological arena. As a result, improved understanding of chemical reactions and interactions at film surfaces and interfaces is required for the design and implementation of new processes and materials that will ensure continuation of device scaling and thus Moore's Law.

The primary goal of this review is to highlight some of the most important surface reactions that drive developments in microelectronic device fabrication. The reactions discussed are not comprehensive of IC manufacture; instead, they have been selected to demonstrate the importance of surface/interface reactions and interactions in the development of new materials, processing sequences, and process integration challenges. Specifically, we focus on surface reactions related to surface cleaning/preparation, semiconductor film growth, dielectric film growth, metallization, and etching (dry and wet). Where appropriate, we describe current challenges and future needs in these areas.

SURFACE CLEANING AND PREPARATION

Device performance, yield, and reliability are degraded by the presence of contamination on a film or substrate surface. The decrease in feature size and spacing to generate more densely packed arrays of device features, combined with an increase in chip size to enhance circuit complexity, have reduced the allowable chemical and particulate surface impurity levels substantially, to fractions of parts per billion. Therefore, the requisite surface cleanliness has become increasingly critical and difficult to attain. Current cleaning processes in IC manufacturing involve both wet (liquid) and dry (generally plasma) cleaning and surface conditioning.

Liquid (Wet) Cleaning and Etching

Approximately 30% of the nearly 800 steps in IC manufacture are cleaning and surface preparation operations; the wet cleaning processes are usually categorized as preprocess or postprocess (5).

Although the wet formulations used have been modified somewhat over the years and various alternatives proposed, the RCA cleaning sequence developed by Werner Kern more than 45 years ago has demonstrated durability and effectiveness; it therefore remains the primary cleaning procedure in IC manufacture (6–8). The reader is referred to comprehensive reviews that discuss the importance and development of liquid cleaning in the semiconductor industry (5, 9). In this review, we focus on the most extensively studied reactions used to clean Si- and SiO_2-based surfaces.

HF-SiO_2 surface reactions. An important part of surface cleaning and conditioning is the removal of oxide layers that are present before the cleaning process or created by the individual cleaning steps. In the case of SiO_2, hydrofluoric acid-based (HF) solutions have removed these layers for more than 50 years; indeed, HF remains an integral part of cleaning procedures in current IC fabrication. The overall chemical reaction occurring on the surface of SiO_2 can be described as:

$$SiO_2(s) + 6HF(l) \rightarrow H_2SiF_6(aq) + 2H_2O. \quad 1.$$

However, aqueous HF is a weak acid, and the solution chemistry is complex, as many hydrogen fluoride species may be present. In the 1960s, the only species detected in dilute (<1 M) HF were HF and HF_2^-; the equilibria can be described by (10):

$$H^+ + F^- = HF \quad 2.$$

$$HF + F^- = HF_2^-. \quad 3.$$

Subsequently, it was recognized that HF can dimerize to form H_2F_2, and in more concentrated solutions, higher ionic complexes such as $H_2F_3^-$ can exist (11).

This already complex HF aqueous chemistry becomes even more complicated when HF comes into contact with SiO_2 surfaces. For instance, SiO_2 etch rates are distinct for each chemical moiety in solution (12), and SiO_2 films formed by different methods [e.g., thermal oxidation of silicon, chemical vapor deposition (CVD), plasma-assisted CVD] or containing dopant (e.g., boron, phosphorus) etch at different rates in the same HF solution.

In addition, the etch rate increases with HF concentration (12–14). However, the relationship between etch rate and either oxide properties (due to the oxide formation method) or HF concentration is currently not understood at a fundamental level. Early studies reported that the SiO_2 etch rate is linearly proportional to the HF and HF_2^- concentrations but is not related to the F^- concentration at any pH. As a result, the following reactions were proposed:

$$SiO_2 + 4HF = SiF_4(ad) + 2H_2O \quad 4.$$

$$SiF_4(ad) + 2F^- = SiF_6^{2-} \quad 5.$$

$$SiF_4(ad) + HF_2^- = HSiF_6^-. \quad 6.$$

The SiO_2 etch reaction rate was believed to be proportional to the HF_2^- concentration but modified by a catalytic effect provided by hydrogen ions. A first order reaction offered the most appropriate fit to experimental data for HF solutions <2 M (15, 16).

Because of the lack of fundamental understanding of these etch reactions, especially in HF solutions >2 M, etch rate data are normally fit to analytical relationships that offer no particular insight into the specific reactions occurring (17).

The bond directionality of SiO_2 polymorphs may introduce further complications to the surface reactions. For example, vitreous silica and silicon dioxide films etch rapidly in HF solutions, whereas coesite etches only slightly, suggesting that a specific silica surface structure may be

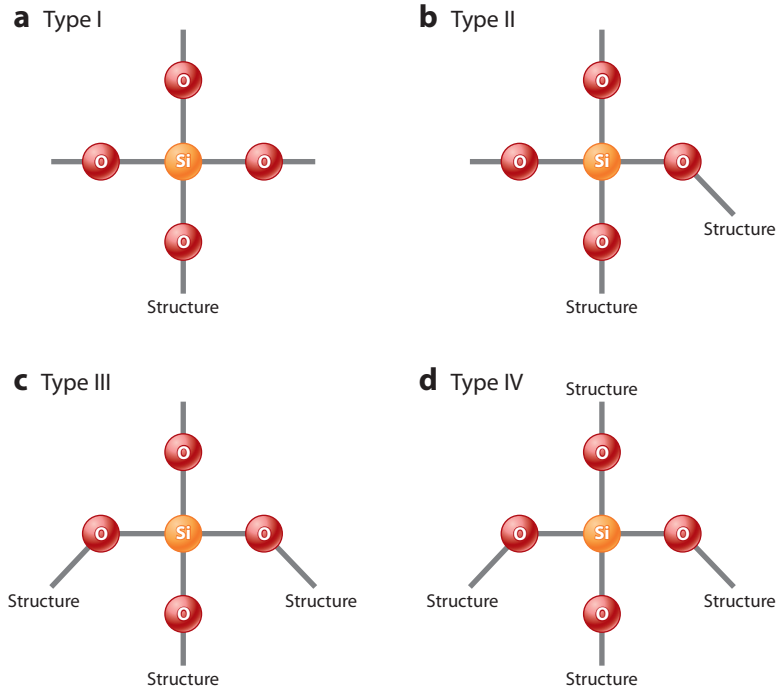

Figure 1

Four possible surface exposures of the silica tetrahedron, designated (*a*) type I; (*b*) type II; (*c*) type III; (*d*) type (IV); "structure" indicates bonding to the bulk silicon oxide layer (19). Adapted from Monk DJ, Doane DS, Howe RT. 1993. A review of the chemical reaction mechanism and kinetics for hydrofluoric acid etching of silicon dioxide for surface micromachining applications. *Thin Solid Films* 232:1–12, with permission from Elsevier.

necessary to initiate the HF etching reaction (18). Moreover, SiO_2 films that have been annealed at high temperatures, and thus densified, etch more slowly in a particular HF solution than do unannealed films. These observations have been rationalized by proposing the four types of surface exposures shown in **Figure 1** (19).

On an open rough surface where etching is enhanced, mostly silica structural types I, II, and III are present. Monk et al. (19) assumed that during etching, types II and III exhibit replacement of OH by F and that nucleophilic attack by hydroxyl ions creates silanol species on the SiO_2 surface.

Similarly, a mechanism of vitreous SiO_2 etching in HF solutions has been proposed (17) (**Figure 2**) in which SiF units replace SiOH units. For a nucleophilic substitution reaction, a nucleophile must approach the electrophile from the side opposite that of the leaving group. When an SiOH group is bound to three oxygen atoms from the SiO_2 matrix, approach of a nucleophile from the matrix side is not possible. Thus, the first reaction step was proposed to be elimination of OH^- and H_2O from the surface to form the reactive intermediate d in **Figure 2**. After elimination of both OH^- and H_2O, structure d can react with three different nucleophiles; reaction with HF_2^- or possibly H_2F_2 will result in reaction product e, the SiF unit. The measured reaction rate will be the product of the elimination and the addition reactions.

After SiF unit formation, the reaction can proceed rapidly. Three subsequent nucleophilic substitution reactions will free the SiF unit from the SiO_2 matrix and return the surface to its initial form in which SiF can replace SiOH to continue the etching process (**Figure 3**).

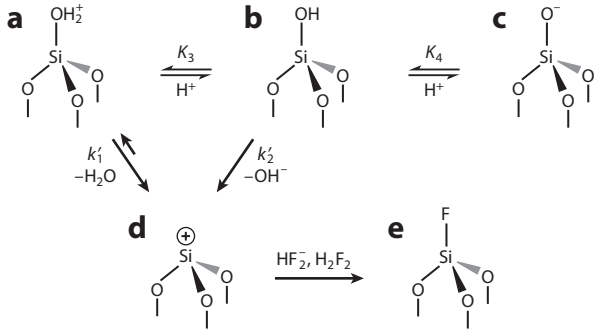

Figure 2

Proposed reaction mechanism of the rate-determining reaction step of the dissolution of SiO_2 in HF solutions: replacement of the SiOH unit by an SiF unit. Adapted with permission from Reference 17, copyright © 2000 American Chemical Society.

Based on the stability of the Si–F bond (~6 eV according to Reference 20), it was believed that HF etching of SiO_2 would yield F termination of Si after the silicon oxide was removed. However, HF etching of SiO_2 leads to hydrogen passivation of the surface (21) even though the bond strength of Si–H is only ~3.5 eV. Recognition of the high polarity of the Si–F bond led to the realization that this bond causes bond polarization of the associated Si–Si back-bond, thereby allowing HF attack of the back-bond, as illustrated in **Figure 4*b*** (22). This kinetically favorable pathway results in the release of stable SiF_x species into the solution, leaving Si–H on the surface, as shown in **Figure 4*c***. The validity of this proposed pathway was consistent with first principles molecular orbital calculations of the activation energies of these types of reactions on model compounds (21).

Selective etch of borophosphosilicate glass/thermally grown silicon oxide using fluorine-based chemistries. State-of-the-art ICs employ SiO_2 doped with B, P, or both to form borosilicate glass, phosphosilicate glass, or borophosphosilicate glass (BPSG) films, respectively, to attain specific material properties (23). P-doped films generally etch faster, and B-doped films etch slower, than undoped SiO_2 owing to differences in electron density at the P or B sites, and the etch rate varies with P/B concentration (24). Because of these differences, it is critical to formulate etch solutions to achieve selective etching of these films. Electron donation from P enhances etch rates via reaction of a hydroxyl group with F from various fluorinated species. Thus, specific

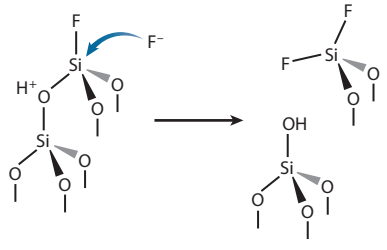

Figure 3

One of the nucleophilic substitution reactions on an SiF_x ($x = 1$, 2, or 3) unit that will result in the removal of the SiF unit from the SiO_2 matrix. Adapted with permission from Reference 17, copyright © 2000 American Chemical Society.

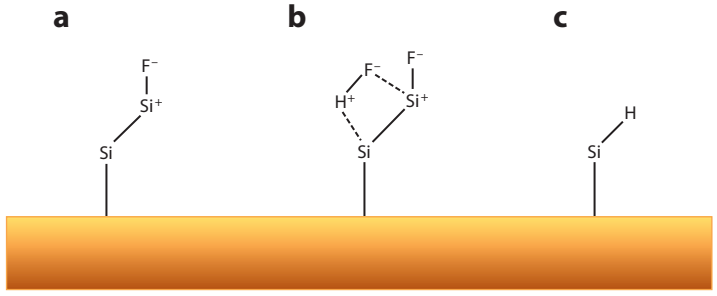

Figure 4

H passivation of silicon surfaces where SiO_2 is etched from the surface using HF solutions (20). Adapted with permission from Springer Science+Business Media.

etchant species or etch conditions can be used to promote preferential interactions with certain bonding structures in doped oxides and thereby tailor etch selectivity to establish control during cleaning/etching steps.

Recently it was demonstrated that a selectivity, here defined as the etch rate (ER) of one material relative to that of another material, of the BPSG etch rate in relation to the thermally grown silicon oxide (TOX) ER of close to one could be achieved by manipulating the etchant chemistry. The use of organic fluoride-based salts in aqueous/organic solvent solution mixtures can yield etch selectivity <1.9 for TOX relative to BPSG films (25).

To improve control of the chemical species formed in solution, fluorine-containing tertiary amine salts were used such that the choice of anion dominated the solvent properties. As previously noted, a plausible mechanism for reaction of HF with SiO_2 involves a two-step reaction: protonation of a surface oxygen atom bonded to a silicon atom (to release OH^- and H_2O from the surface to form a reactive intermediate) followed by nucleophilic attack of Si by HF_2^-. In the reaction of $HF_2^-/H_2F_3^-$ anions with SiO_2, the polar component of the solvent should stabilize the ionic intermediate, and the protic component should solvate the leaving groups (OH- or H_2O). Because the ER for TOX and BPSG is low in organic solvents such as dimethylsulfoxide (DMSO) and tetrahydrofuran (THF), these polar aprotic solvents cannot solvate the leaving group, and a more polar component is needed. To address these issues, aqueous/organic salt mixtures were invoked. **Figure 5** demonstrates the ER variation for TOX and BPSG as well selectivity for these films in tetrabutylammonium bifluoride (TBABF) and tetrabutylammonium dihydrogen trifluoride (TBADT)/water solutions. This approach permits an ER selectivity of BPSG to TOX of two to be readily achievable at a 0.5 M concentration of these salts in water.

Clearly, despite decades of research on HF chemistry and surface reactions during film etching and cleaning, only limited fundamental understanding of the etch mechanism and thus etch selectivity of different films with specific chemical moieties in HF solutions exists. Such information is critical for future device/IC fabrication to achieve requisite selectivities and thus ensure the process control necessary for smaller device and film dimensions.

Vapor Phase Removal of Metal Contaminants from Surfaces

Nearly all HF-based cleaning approaches depend on etching or undercut of a layer of SiO_2 to lift off surface impurities/residues. Due to reduced film thicknesses and device sizes in future IC generations, such approaches require either greatly improved selectivities during cleaning or alternative methods to achieve impurity/residue removal in which cleaners do not react with existing films/surfaces.

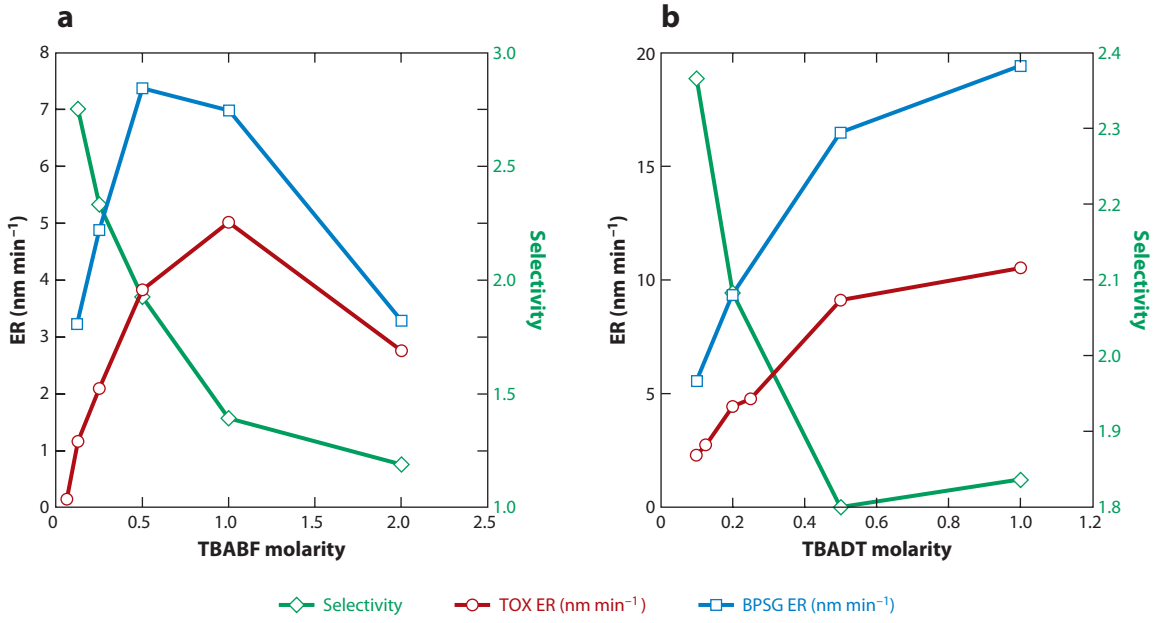

Figure 5

Etch rate (ER) and selectivity variation for thermally grown silicon oxide (TOX) and borophosphosilicate glass (BPSG) in tetrabutylammonium bifluoride (TBABF)/water (*a*) and tetrabutylammonium dihydrogen trifluoride (TBADT) /water (*b*) solution (25). Adapted with permission of ECS–The Electrochemical Society.

Because of integration difficulties encountered when using both wet and dry processes and due to the increased aspect ratios of small structures present on current and especially future devices and circuits, considerable interest in vapor phase removal of contaminants has developed (26, 27). Typical approaches have used UV/ozone and/or plasmas for organic contaminant removal and/or UV/Cl_2 for removal of certain metals. Removal of metals is particularly difficult because it requires the formation of volatile metal compounds by reaction of the metals with reactive chemical species that can also react with underlying films or substrates. One approach to mitigating such reactions with other films involves the complexation of metals with chemical ligands. For instance, selective vapor-phase cleaning/etching of copper and iron from surfaces has been reported (28, 29). In particular, 1,1,1,5,5,5- hexafluoro-2,4-pentadione (H^+hfac) vapors were used to chemically remove copper films, a reaction in which H^+hfac interacts with the surface-bound copper to form a volatile metal chelate. These studies demonstrated clearly that the ability to remove or etch copper depends critically on the chemical state of the copper.

The overall chemical reaction for Cu^{II} with H^+hfac involves the creation of a volatile chelate accordingly to the reaction:

$$2H^+\text{hfac} + \text{CuO} = \text{Cu(hfac)}_2 + \text{H}_2\text{O}. \qquad 7.$$

However, reaction of Cu^{II} with H^+hfac results in copper disproportionation:

$$\text{Cu}_2\text{O} + 2H^+\text{hfac} = \text{Cu}^0 + \text{Cu(hfac)}_2 + \text{H}_2\text{O}. \qquad 8.$$

No reaction was observed between H^+hfac and Cu^0. Therefore, if Cu^I is present on the surface (from Cu_2O for example), both Cu^0 and Cu^{II} are generated as a result of H^+hfac reaction; Cu^{II} is removed by volatilization, but Cu^0 is not, eventually resulting in a buildup of Cu^0 and a

termination of the copper removal process. These results clearly demonstrate that if controllable and reproducible processes are to be established, it is often critical to know the oxidation state of surface species involved in cleaning and etching reactions and therefore the specific chemical reactions that occur.

Interfacial Interactions in Residue Removal

To enable anisotropic etching, a thin fluorocarbon layer is deposited on the sidewalls of features during etch, thereby inhibiting lateral etching and ensuring dimensional control (30, 31). A primary challenge in IC fabrication is residue removal after fluorocarbon-based plasma etching of Si-based films. In addition, fluorine atoms and fluorocarbon ions bombard the photoresist surface, causing the formation of a carbonaceous, fluorinated crust (32–34). Prior to subsequent processing steps, this sidewall and photoresist/crust residue must be removed. Incomplete removal of the residue can result in poor adhesion of subsequent film layers, material contamination, and inadequate feature size control (7, 35, 36).

The low surface energy and chemical inertness of fluorocarbon materials prevent most traditional aqueous chemistries from being completely effective in residue removal (7, 37). Furthermore, the plasma environment can cause strong adhesion of residues to the underlying layer and thus change the existing interfacial tension. The chemical structure of the residue is also strongly process- and equipment-dependent, which complicates the development of removal chemistries applicable to a broad array of plasma etch formulations and conditions. Little information is available regarding specific reactions/interactions that control residue removal; most studies investigate removal by trial-and-error approaches.

During the cleaning process, the residue to be removed should be physically or chemically separated from the underlying substrate or film without altering the substrate or film properties. This requirement implies that, in addition to the interactions and possible reactions between the cleaning chemistry and residue, interactions such as those due to residue-substrate and cleaning chemistry–substrate are involved in the overall process and must be taken into consideration to achieve effective residue removal. Interactions between the solvents and films to be dissolved/removed are in part established by the characteristic parameters of the solvent and the surface. Solvents can alter the interactions between various surfaces by changing wetting properties of the surface, promoting separation of surfaces, or affecting adhesion between surfaces.

The cleaning efficiency of solvent-based cleaning solutions and correlation to solvatochromic parameters have been reported (37). Owens-Wendt analysis has been used to evaluate the interactions between fluorocarbon-based residues, substrates, and solvent properties; both the effect of the solvent and the addition of ionic solvent modifiers were considered. Chemical similarity was established between solvent and surface by matching polar and dispersive components to allow initial evaluation of cleaning mixtures for post-plasma-etch residue removal. Addition of ionic salts to deionized water or *N*-methylpyrrolidone (NMP) decreases the overall surface tension and alters the distribution of polar and dispersive components that account for film-surface interactions. Fluoride-containing salts exhibited the opposite behavior in water and NMP, which was attributed to differences in solvation and hydrolysis of the salt. Estimations of the change in separation energy between the residue and the substrate as a function of specific cleaning solution correlated well with observed residue removal.

Interfacial interactions are significant throughout most process steps in IC manufacture; further details can be found in Reference 38. Because of the numerous interfaces in devices/structures, device performance can depend on the energy created and released at these interfaces; however, relatively little fundamental information is currently available.

Plasma Cleaning and Surface Preparation

Plasma etching for photoresist removal and cleaning is performed routinely in IC manufacture and includes removal of bulk photoresist and residues at the bottom and sidewalls of etched features as well as predeposition surface cleaning and conditioning.

Detailed discussion of photoresist removal can be found elsewhere (39); in this review we provide general information about the surface reactions involved.

Plasmas or glow discharges used in IC processing are weakly ionized gases composed of electrons and positive and negative ions, radicals, and neutral species in ground and excited states. The plasma is formed by applying an electric field to a low-pressure gas, thereby causing ionization, dissociation, and excitation. Owing to the complexity of the plasma and the bombardment of substrates by electrons, ions, neutrals, and photons, precise definition of surface reactions is difficult at best (40).

The simplest chemistry used for photoresist stripping is an oxygen plasma that ashes photoresist away; this process was first implemented in the early 1970s. The basic ashing reaction of oxygen-based plasma with photoresist polymers is oxidative and can be described simply as (41, 42):

$$C_xH_y + O^\bullet = CO + CO_2 + H_2O. \qquad 9.$$

The primary surface reactions involve the abstraction of H from the photoresist by either $O^\bullet$ or $F^\bullet$ (fluorinated gases are often added to the plasma atmosphere to enhance photoresist stripping rates); the broken bond is therefore susceptible to rapid attack by $O^\bullet$ or $^\bullet OH$, forming volatile products as indicated in Equation 9.

Small additions of N_2 can promote the dissociation of O_2, and N_2 will react with C on the resist surface to form CN; in both cases the photoresist stripping rate increases (43).

Photoresist can be removed by reaction of C–H bonds with $H^\bullet$ generated from a hydrogen plasma to form H_2 and generate free radical sites that react further to fragment the photoresist. In addition, $H^\bullet$ reacts with both double and triple bonds in the photoresist to form saturated hydrocarbons that can easily desorb from the surface. Irrespective of the particular etchant used for plasma-assisted removal of photoresist, the specific chemical reactions have been difficult to define, and it has been especially difficult to quantify the synergistic effects that are observed with ion, photon, and electron bombardment.

FILM GROWTH AND DEPOSITION

Electronic device scaling to nanometer dimensions has greatly accelerated development of thin film deposition technologies and equipment, precursors employed and implementation of new film materials and process sequences. Film growth requires atoms or molecules to be transported to a surface where they are incorporated into a film. This process normally follows several steps. First, a molecule adsorbs on the surface either by physisorption (adhesive force is essentially a van der Waals interaction) or chemisorption (strong covalent bonds are formed between the molecule and the surface). Once molecules are on the surface, they diffuse until they reach a reactive site where they can react with other surface species, release products, and form a film. The mobility of surface species is higher on metallic and semiconducting surfaces, where bonding is generally less directional, and rather limited on dielectrics, where highly directional covalent bonds can immobilize a molecule after chemisorption. These unique characteristics have been employed to develop deposition techniques that involve physical or chemical interactions. This brief review focuses on chemical methods of film deposition that involve surface reactions.

Chemical Vapor Deposition

CVD involves deposition of film materials from the vapor phase by means of chemical reactions. Initial use of CVD in IC processing involved deposition of insulators such as SiO_2 and Si_3N_4 and epitaxial semiconductor layers such as silicon (44). The silane surface reaction has been one of the most widely investigated over the past few decades (44–54). Differences in reaction paths, activation energies, and reaction orders of SiH_4 and H_2 have been reported as a result of the complexity of the surface reactions involved and the limitations of in situ surface measurements; these observations emphasize the current lack of understanding and thus the importance of better defining surface reactions in such processes (51). Despite these limitations, CVD has evolved and developed over the past 50 years, which has resulted in extensive use of this technique in IC manufacture. Many excellent reviews and monographs on CVD have appeared that discuss the variety of deposition conditions, deposition tools, and mechanistic considerations for different films and substrates (55–62). In this review we focus on selective CVD, specifically selective deposition of tungsten owing to its inherent and critical reliance on surface reactions.

Selective deposition of tungsten. Metallization to establish electrical contact to devices as well as to interconnect billions of devices (e.g., transistors, resistors, capacitors) is a required step in IC fabrication. Limitations of aluminum metallization in the 1980s included the inability of aluminum to withstand temperatures greater than ~500°C, which precluded high-temperature process sequences, and the metallization's inadequate step coverage owing to film formation by sputtering. To overcome these problems, CVD of tungsten was introduced. A key feature of W CVD is that the deposition is surface chemistry controlled and thus can in principle be selective, thereby precluding the need for a separate patterning step. The thickness and physical film structure of W deposited by the silicon reduction of WF_6 is dependent upon silicon surface preparation and native oxide characteristics (63–64). Nucleation of W growth is inhibited on insulator surfaces (65–67), although nucleation can be promoted on SiO_2 if broken bonds are present at or impurities are incorporated into the surface. However, adhesion of CVD-grown W on SiO_2 is often inadequate and requires high-temperature annealing or the deposition of polysilicon and/or metals onto the SiO_2 surface (65).

Several techniques can be used to selectively deposit W on silicon, namely silicon reduction of WF_6 with and without hydrogen addition as well as reduction of WF_6 with silane (54, 65, 68–71).

Tungsten deposited by the reduction of WF_6 with silicon occurs through etch and deposition reactions. Moreover, the balanced equation for the reaction shows that for every two tungsten atoms deposited, three silicon atoms must be removed:

$$2WF_6 + 3Si = 2W + 3SiF_4. \quad 10.$$

If an additional (to SiF_4) volatile product such as SiF_2 is formed, the equilibrium shifts further toward etching,

$$WF_6 + 3Si = W + 3SiF_2, \quad 11.$$

where the branching between these two reaction pathways is temperature dependent.

The kinetics of these reactions has been extensively studied, and although the reaction products SiF_2 and SiF_4 are clearly distinct from each other, both consist of fast and slow components (72–74). In References 72–74, it was speculated that for the fast component the product is emitted immediately when WF_6 reaches the surface and creates high local concentrations of fluorine atoms. However, after the concentration of fluorine atoms dissipates by diffusion, the formation of SiF_2 or SiF_4 requires regrouping of the fluorine atoms (72, 74). Also, no deposition is observed after a limiting deposit thickness is reached. This is a serious limitation when controllable deposition

with thicknesses higher than several tens of nanometers and limited Si etching is required. To overcome this problem, the growth of tungsten on Si in the presence of hydrogen was suggested:

$$WF_6 + 3H_2 = W + 6HF. \quad 12.$$

This reaction is reported to be a function of H_2 partial pressure; the rate-limiting step is dissociation of hydrogen on the surface.

SiH_4 has also been extensively studied as a reducing agent to replace Si in reaction with WF_6 and to avoid extensive etching of bulk silicon as well as limited thickness of deposited metal (67, 70, 77). However, the reaction is complex, and a large number of possible reaction pathways exist:

$$xSiH_4 + yWF_6 = yW + xSiF_4 + (6y - 4x)HF + (4x - 3y)H_2, \quad 13.$$

where $4x \geq 3y \geq 2x$. These chemistries are selective for tungsten.

Molecular beam/mass spectroscopy experiments (76, 77) showed that the major reaction pathway in this case is hydrogen production through dissociation of silane; silane reacts with WF_6 to produce H_2 and SiF_4 and to deposit silicon. With silicon residing on the tungsten surface, WF_6 molecules can react again through the silicon-reduction reaction, which leads to deposition of additional tungsten; however, this reaction is not dependent on the bulk silicon. In this case, after the deposition reaction is initiated, the substrate surface has a minimal effect on the chemistry of the tungsten deposition.

Atomic Layer Deposition

For nanoscale device structures with high aspect ratios, thin (<10 nm) conformal films must be deposited. As a result, atomic layer deposition (ALD) has generated much interest. ALD is a variation of CVD that allows controlled film deposition layer by layer at the atomic level by taking advantage of self-limiting surface reactions; this is commonly achieved by exposing a surface to alternating fluxes of reactive precursors. Although ALD originated in the early 2000s, the analogous technique of atomic layer epitaxy (ALE) was previously invoked to enable uniform thin film deposition over large areas (78–80). Initial applications for ALD were limited to the deposition of epitaxial layers of II-VI or III-V semiconductors for display devices because its inherently low growth rate was a major limitation for other applications (78, 81). However, due to device scaling, the demand for thin (<10 nm) amorphous or polycrystalline films has grown enormously. Thus, ALD has found applications in metal oxide semiconductor field effect transistors (MOSFETs) and high-density memory devices as a method to grow high dielectric constant gate oxides in MOSFET structures, contact layers, and diffusion barriers for copper or other metallization (45, 82, 83).

The sequential self-limiting surface reactions in ALD allow atomic layer control and conformal film deposition. A schematic for a generic ALD process is shown in **Figure 6**.

Most ALD processes are based on binary reaction sequences (**Figure 6**) in which two surface reactions occur and deposit a binary compound film. After creation of reactive surface sites, perhaps by introducing OH groups, a gaseous precursor is dosed onto the surface. The precursor must not react with itself or in the gas phase, nor should it decompose on a surface without reactive sites. Because the number of surface reactive sites is finite, this first reaction is self-limiting; excess precursor that did not react with surface sites is purged from the reactor. The surface is then exposed to the second reactant. This reaction is also self-limiting because this species can react only with the chemisorbed first reactant to form a single molecular film layer; by-products of the reaction must be volatile so that they can be removed easily. Again, excess reactant is purged from the reactor. This low–deposition rate, atomic-scale, self-limiting deposition approach of ALD

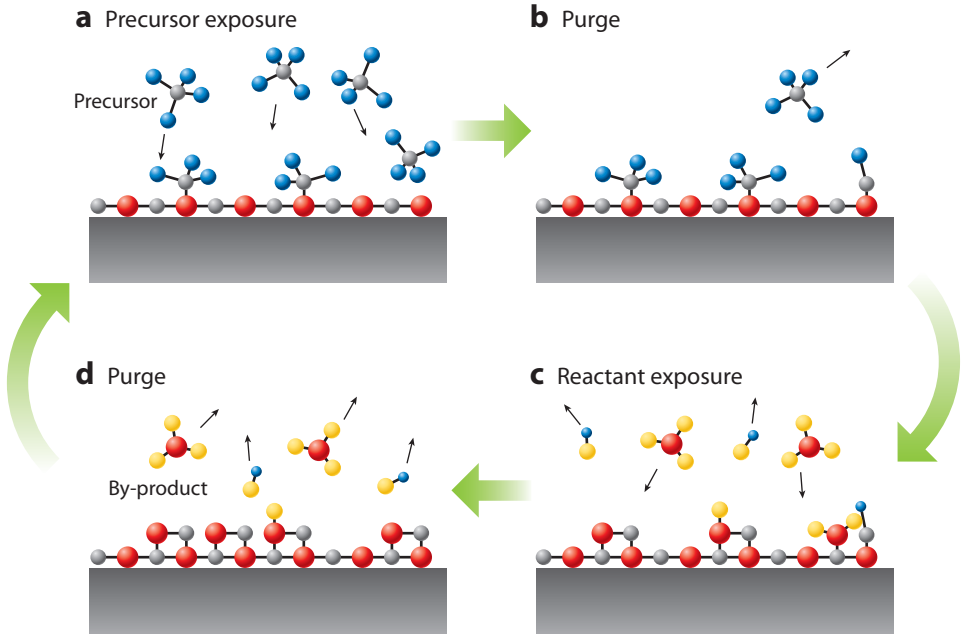

Figure 6

Schematic of an atomic layer deposition film growth process (82). Adapted from Kim H, Lee H-B-R, Maeng W-J. 2009. Applications of atomic layer deposition to nanofabrication and emerging nanodevices. *Thin Solid Films* 517:2563–80, with permission from Elsevier.

differs from that of CVD and yields excellent film conformality and thickness control. An example of the formation of a thin hafnium oxide gate dielectric by ALD is described below.

Surface reactions in hafnium oxide atomic layer deposition. Hafnium oxide deposition by ALD uses $HfCl_4$ and H_2O as precursors (84–86). The sequence of binary chemical reactions that result in film deposition can be described by

$$\text{Hf–OH}^* + \text{HfCl}_4 = \text{Hf–O–HfCl}^* + \text{HCl} \qquad 14.$$

$$\text{Hf–Cl}^* + \text{H}_2\text{O} = \text{Hf–OH}^* + \text{HCl}, \qquad 15.$$

where the asterisk denotes surface species that may have both Cl and OH groups attached. For instance, Hf–Cl* has an active Cl atom as well as additional hydroxyl groups and chlorine atoms bonded to Hf atoms (87).

Detailed reaction mechanisms have been investigated using density functional theory and computational results compared with experimental data (88). The potential energy surfaces for both half reactions indicate that these reactions involve intermediate complexes formed between the precursors and surface active sites; both intermediates are physisorbed.

Reaction kinetics approaches and kinetic Monte Carlo methods have been used to evaluate the effects of intermediate formation, the local chemical environment on the reaction rate parameter, possible surface reactions, and diffusion (88). A mechanism was proposed to explain several experimentally observed deposition phenomena such as the formation of less than one monolayer per cycle and the dependence of film growth rate and residual chlorine concentration on process temperature (88).

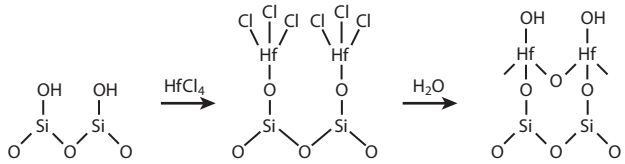

Figure 7

Idealized scheme of the first HfO_2 atomic layer deposition cycle on hydroxylated SiO_2 using $HfCl_4$ and water (20). Adapted with permission from Springer Science+Business Media.

Figure 7 shows an idealized reaction scheme for HfO_2 formation on a hydroxylated silicon oxide surface. This scheme is simplistic and thus does not account for possible reactions of precursor with more than one hydroxyl group, incomplete hydroxyl consumption, steric hindrance, or cross-linking of metal ions through oxygen bridges.

Two nonidealities are frequently encountered when depositing high-*k* dielectrics onto silicon surfaces: nonlinear growth and substrate oxidation (20). Nonlinear growth was observed when attempting to fabricate atomically sharp Si/high-*k* interfaces by depositing high-*k* dielectrics onto oxide-free hydrogen-terminated Si. As shown in **Figure 8*a***, at 300°C and using $HfCl_4$ and H_2O as precursors, the amount of HfO_2 deposited is initially not proportional to the number of ALD cycles (89).

In this system, initial growth proceeds slowly until a linear growth regime is reached after ~50 cycles. The first ALD cycles deposit fewer metal-containing groups on the hydrogen-terminated surface than are observed after a metal oxide film is formed. Such delayed nucleation is characteristic of undesirable island growth as confirmed by transmission electron microscopy

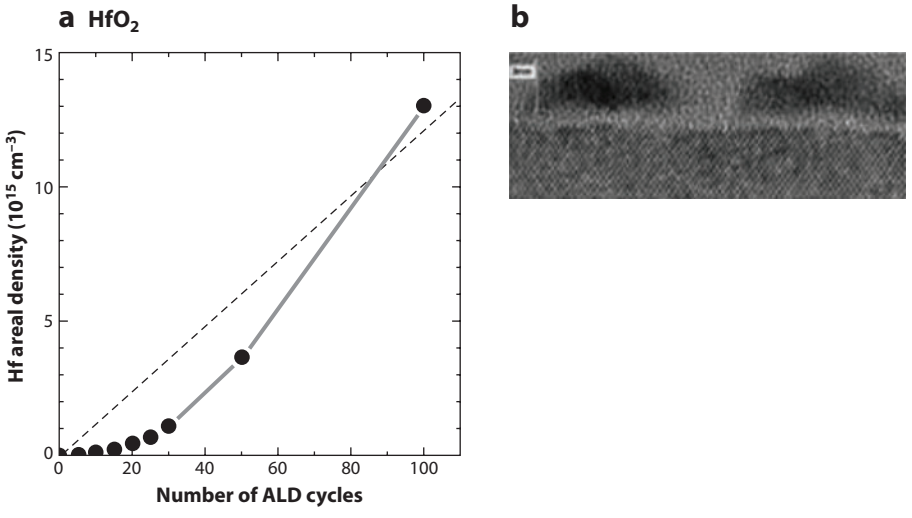

Figure 8

(*a*) Areal density of Hf ions as a function of the number of atomic layer deposition (ALD) cycles for HfO_2 growth on hydrogen-terminated Si(100) at 300°C. The dotted line approximates the density expected for uniformly nucleated films. Adapted from Reference 89 with permission from Springer Science+Business Media. (*b*) Transmission electron microscopy image from the same growth system (precursors $HfCl_4$ + H_2O) (90). Reprinted from Gusev EP, Cabral C, Copel M, D'Emic C, Gribelyuk M. 2003. Ultrathin HfO_2 films grown on silicon by atomic layer deposition for advanced gate dielectrics applications. *Microelectron. Eng.* 69:145–51, with permission from Elsevier.

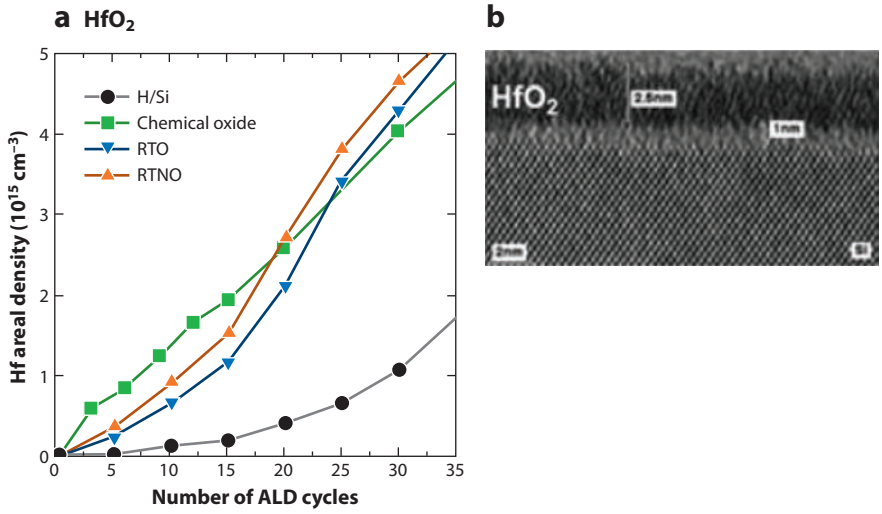

Figure 9

(*a*) Areal density of hafnium ions as a function of the number of atomic layer deposition (ALD) cycles for high-*k* growth on oxidized Si(100) at 300°C [precursors $HfCl_4$ + H_2O (data from 89)]. Reprinted with permission from Springer Science+Business Media. (*b*) Transmission electron microscopy image of HfO_2 growth on thermal oxide (90). RTNO, rapid thermal oxidation in 60% O_2/40% NO atmosphere; RTO, rapid thermal oxidation. Reprinted from Gusev EP, Cabral C, Copel M, D'Emic C, Gribelyuk M. 2003. Ultrathin HfO_2 films grown on silicon by atomic layer deposition for advanced gate dielectrics applications. *Microelectron. Eng.* 69:145–51, with permission from Elsevier.

(**Figure 8*b***). The films deposited on hydrogen-terminated Si produced high leakage currents measured between the channel and gate electrode (90). To improve ALD nucleation, oxidized/hydroxylated silicon surfaces have been used instead of inert hydrogen-terminated silicon surfaces. Under these conditions, growth proceeds nearly linearly (**Figure 9**), indicating essentially uniform nucleation (89, 91).

Continuous HfO_2 layers with high breakdown strength were formed at thicknesses as low as ~2 nm (**Figure 9*a***). Initial growth rates for HfO_2 film deposition using $HfCl_4$ and water as precursors increase with the following surface preparation conditions: H/Si ≪ thermally grown SiO_2/Si < wet-chemically grown SiO_2/Si (89). These results indicate that nucleation correlates with substrate hydroxyl group density and supports the assumption that hydroxyl groups are the primary reaction sites for $HfCl_4$ molecules (**Figure 7**).

PLASMA ETCHING

Plasma processing is used extensively in IC manufacturing. After plasma-based dissociation of etchant molecules to form reactive etchant species (e.g., neutrals, radicals, ions), plasma etching occurs through a series of surface steps: reactant adsorption, reaction, and volatile product desorption. Anisotropic etching occurs by the acceleration of positive ions into the etching surface to enhance the rate of surface reactions and thereby supply directionality to the pattern formed. Isotropic etching is due to neutral reactive species such as free radicals that etch at the same rate in all directions. For nearly three decades, most film materials used in IC fabrication have been etched using halogen-based plasma chemistries (30, 92–97).

Selective Etch of SiO_2 and Si

In addition to generating anisotropic patterns, plasma etching must be selective with regard to the films or substrates beneath the material being etched. For example, when etching contact holes through a dielectric such as SiO_2, etching of the underlying Si or other material must be avoided to ensure reliable device properties (98). Furthermore, for high-density device packaging, through silicon vias (TSV) technology is used to etch entirely through a silicon wafer (~350 μm) while maintaining anisotropy. It has been well known for more than 30 years that the etch rate ratio of SiO_2/Si with CF_4 can be increased by addition of hydrogen to a CF_4 plasma or by replacing CF_4 with a higher-order fluoroalkane such as C_2F_6 or C_3F_8 (99). Simultaneous plasma polymerization and plasma etching causes the increase in etch rate ratio or selectivity. The added H_2 gas scavenges F atoms, thereby shifting the chemistry from a primarily etching chemistry (pure CF_4) to a polymerizing chemistry (CF_4+ H_2); analogous results are observed with the use of higher-order fluoroalkanes that are polymerizing gases. The polymeric film that forms serves as a protective layer to prevent etching of Si, whereas oxygen released during the etching of SiO_2 combines with carbon species from the etch gas to form volatile products such as CO, CO_2, or even COF_2, thereby removing residues from locations where ion bombardment occurs and allowing the SiO_2 etch to continue (98).

Figure 10 is a schematic that indicates surface impingement of plasma species and buildup of sidewall polymer and redeposited material in an etching plasma (31). Owing to the importance of selective etching of SiO_2 in IC fabrication, numerous studies of this process have been published (100).

In an attempt to develop a simplistic but essentially realistic physical/chemical model of SiO_2 selective etching using C_4F_8/Ar/O_2 as the etch gas mixture, the surface layer during etching was assumed to consist of two layers: a reactive layer (a mixture of Si, F, C, and O) and, above it, a

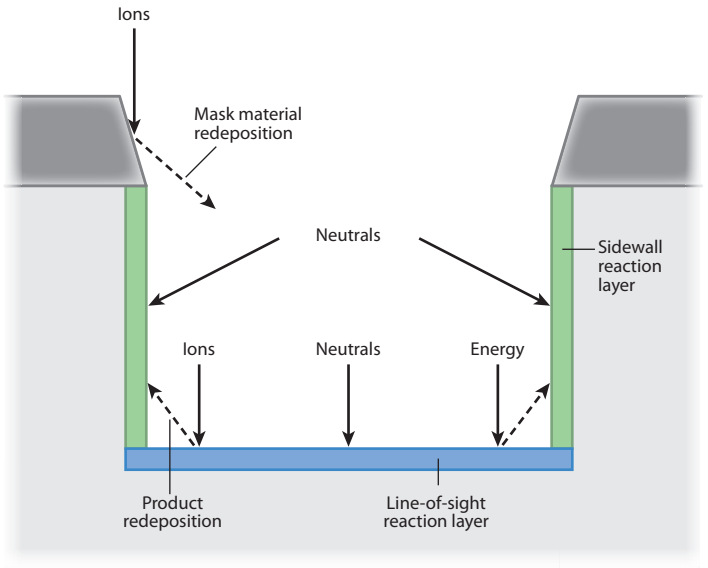

Figure 10

Surface processes leading to residue formation during plasma etching of a via or a trench (31). Adapted from Oehrlein GS, Kurogi Y. 1998. Sidewall surface chemistry in directional etching processes. *Mater. Sci. Eng. R.* 24:153–83, with permission from Elsevier.

C-F polymer layer (101). This top layer inhibits reaction or etching of the underlying film by F generated in the plasma. Results indicated that the formation of polymer layer could thereby greatly reduce the probability of surface reaction. This fluorocarbon polymer acts as a diffusion barrier for the F etchant and a protection layer from ion bombardment.

Although excellent control of selectivity, especially with the thin layers and small structures currently used in IC fabrication, is required, in some situations both high etch rates and selectivity are needed. For many years, SF_6 has been used to isotropically etch silicon (102).

Etchant is generated by plasma-assisted dissociation of the relatively inert SF_6 (103):

$$SF_6 + e^- = S_xF_y^+ + S_xF_y^* + F^\bullet + e^-. \quad 16.$$

Fluorine radicals, assisted by ion bombardment, react with and etch silicon by formation of volatile SiF_4:

$$Si + 4F^\bullet = SiF_4(g). \quad 17.$$

In the closely spaced features that are commonplace in current and future ICs, anisotropic etching is required. As described above, polymer sidewall passivation or protection is used for this purpose. When deep etch processes or high aspect ratio structure generation is needed, a two-step process is implemented, the so-called Bosch process (104).

A short polymer deposition cycle after an etch cycle deposits a fluorocarbon protection layer on sidewalls and at the base (bottom) of the etched feature. Layer formation occurs as a result of fluorocarbon radical generation from dissociation of the C_4F_8 gas followed by polymerization owing to the high reactivity and enhanced adsorption of C and CF_x radicals (free radical polymerization) (103):

$$C_4F_8 + e^- = CF_x^+ + CF_x^\bullet + F^\bullet + e^- \quad 18.$$

$$CF_x^* = nCF_2(\text{fluorocarbon polymer}). \quad 19.$$

The passivation material is then removed from the bottom of the etched feature during the subsequent etch cycle by ion bombardment and fluorine radical reaction, whereas the sidewall passivation layer is left intact because little, if any, ion bombardment occurs on the sidewalls:

$$nCF_2 + F^* = CF_x^* = CF_2(g). \quad 20.$$

A schematic of the two-step etch cycle is shown in **Figure 11**; SF_6 and C_4F_8 are shown as undissociated plasma species simply to indicate the fluxes involved in the etch and deposition steps. This sequence of cycles enables an anisotropic, high-rate silicon etch to be achieved despite the isotropic etch nature of fluorine radicals.

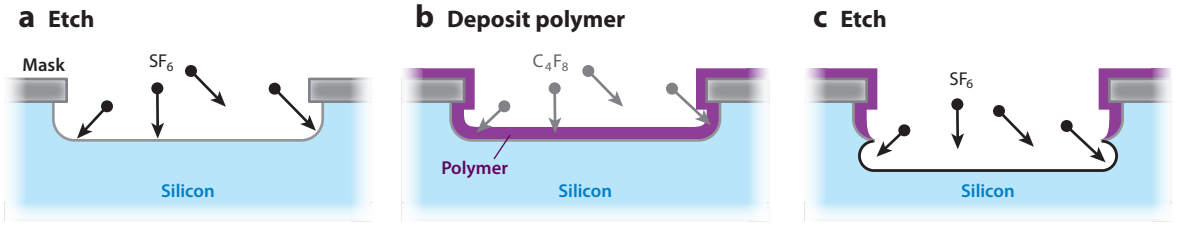

Figure 11

Schematic representation of the Bosch process (105). Adapted with permission from IOP Publishing.

However, the cycling of etch and deposition steps creates periodic nanoscale surface structures known as scallops on the sidewalls of the etched structures. To improve the anisotropy, additional gasses such as oxygen or argon (106–112) have been introduced into plasma atmospheres to alter the surface reactions and thus remove scallops.

Plasma Etching of Copper

More than 15 years ago, Cu interconnection layers replaced Al layers to establish higher device speed. Initially, the transition from patterning Al to patterning Cu was unsuccessful because unlike Al, Cu does not form volatile halogenated etch products at temperatures below 180°C.

These restrictions led to the introduction of damascene technology in 1997 (113). In this approach, an SiO_2 film is patterned and Cu plated into the etched holes (vias). For current and future devices/circuits, this approach to Cu patterning has limitations because the electrical resistivity of Cu plated in these small vias increases rapidly as lateral dimensions decrease below 100 nm because grain growth in the plated films is inhibited (114–117). This obstacle could be overcome in part by the use of copper films with larger grain size. Sputtered or evaporated and annealed films also could be a potential solution (118–120).

To date, chlorine-based plasmas have been used to plasma etch Cu, because surface reactions of chlorine with copper generate copper chlorides that have the highest volatility of any halogen-containing Cu compound. However, the volatility is sufficiently low that high temperatures (>180°C) are needed to effectively desorb Cu chlorides (121–125). To reduce the temperature required, photon-enhanced removal of Cu chlorides at temperatures below 100°C by laser (126), UV (127–133), or infrared radiation (132, 133) has been studied. Recently, a low-temperature (10°C) two-step Cu plasma etching process was reported that is based on a thermochemical analysis of solid-gas volatilization reactions in the Cu-Cl-H system (134). In the first step, the Cu film surface is chlorinated in a Cl_2 plasma at low temperatures to form $CuCl_2$ preferentially relative to CuCl (135). In the second step, a hydrogen plasma is used to convert $CuCl_2$ into a product with improved volatility, presumably Cu_3Cl_3, which is reported to be more volatile than $CuCl_2$ or CuCl (136). Subsequent studies have demonstrated that a pure H_2 plasma can etch a Cu film at these low temperatures (137). This result is unexpected and not easily explained by simple hydrogen reaction with a copper surface because CuH, CuH_2, and other CuH_x species are reported to be less volatile than Cu chlorides. In an H_2 plasma, the Cu surface is exposed to ions, radicals, electrons, and plasma-emitted photons. Comparison of Cu etch results among Ar, He, and H_2 plasmas suggests that in addition to hydrogen atoms, both ion and photon bombardment contribute to the surface etching process. Currently, no fundamental understanding of this surface etch reaction has been established.

Atomic Layer Etching

The continual reduction in feature size and film thickness in ICs increases the sensitivity of device properties to film/surface damage (i.e., chemical bond breakage) and raises the etch uniformity required during patterning processes (138–140). Therefore, etching steps must minimize or eliminate surface and subsurface damage induced by ion, electron, and photon bombardment as well as uniformly remove thin (essentially atomic) layers of material. Such control may be possible if a self-limiting etch process is developed. To realize this goal, a technique similar to ALD has been proposed to achieve layer-by-layer etching. Atomic layer etching (ALE) [also known as plasma atomic layer etching (PALE) or digital etching] (141) is a cyclic process comprising four consecutive steps (**Figure 12**): (*a*) exposure of a surface to an etchant gas that is adsorbed (chemisorption) to form a monolayer; (*b*) evacuation of the chamber so that only the chemisorbed layer of etchant

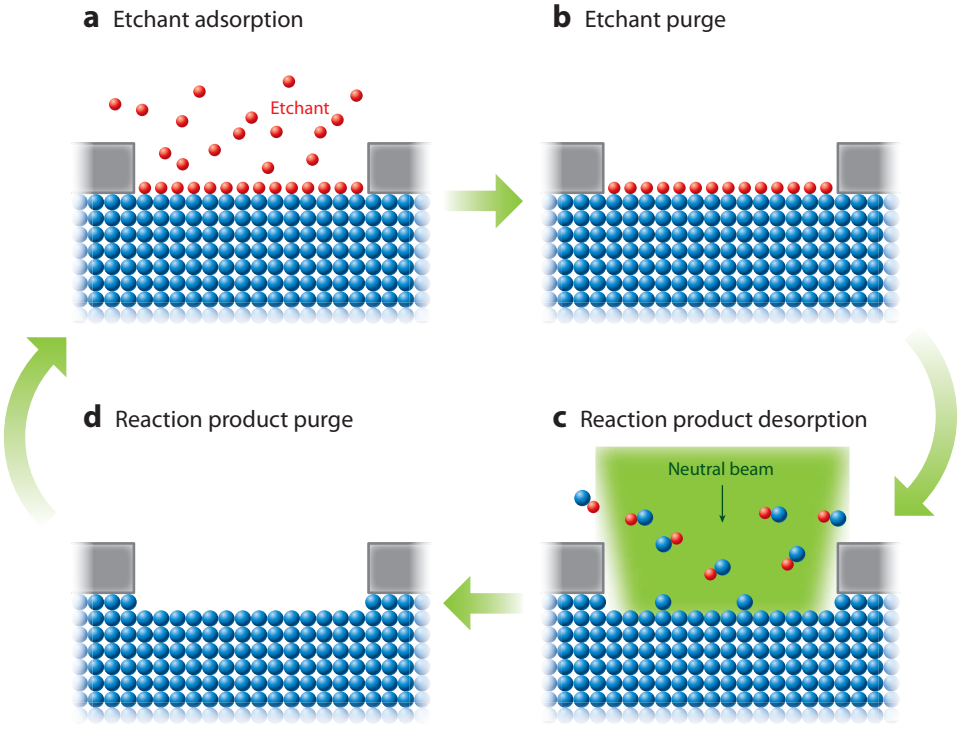

Figure 12

Schematic representation of a four-step atomic layer etching process (142). Adapted with permission from IOP Publishing.

remains, which is necessary to avoid etching by gas-phase species in step *c*; (*c*) surface exposure to an Ar^+ ion beam to cause chemical reaction between the adsorbed gas and the underlying solid to remove a monolayer of solid; and (*d*) evacuation of the chamber to exhaust the reaction products. Completion of one cycle results in the etching of one atomic layer. The cycle can be repeated to etch as many atomic layers as desired (142).

To achieve etching with atomic layer control, the process must be self-limiting with respect to both gas dose in step *a* and ion dose in step *c*. This means that the etchant gas used in step *a* must not react spontaneously with the surface and also that the ions in step *c* need to be inert. In addition, the ion energy must be low enough to prevent surface sputtering and to minimize or eliminate bond breakage in subsurface layers.

Initial applications of ALE to Si etching were reported in the late 1980s and early 1990s. For example, layer-by-layer etching of Si was observed at a temperature of −110°C, where the etch rate depended on exposure of substrates to a downstream fluorine-containing plasma (143). Subsequently, self-limited layer-by-layer etching of Si using alternating chlorine adsorption and low-energy Ar^+ ion irradiation steps at room temperature was demonstrated (144). Further studies were performed to modify and optimize the ALE methodology (141, 145). Specifically, it was determined that an ion dose of 1.163×10^{16} ions cm^{-2} is necessary to remove one monolayer of silicon, that reactions in ALE occur on the picosecond timescale, and that long timescale chemistry (hundreds of milliseconds), which is possible in ion-assisted etching with simultaneous exposure to neutral and ion beams, does not occur in ALE.

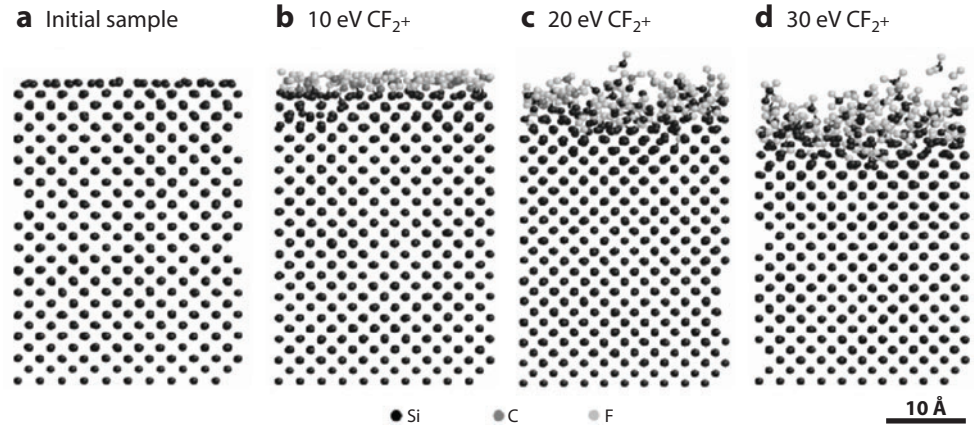

Figure 13

(*a*) Initial Si sample. (*b–d*) The sample after bombardment with CF_2^+ ions of energies of (*b*) 10 eV, (*c*) 20 eV, and (*d*) 30 eV (146). Reprinted with permission from Rauf S, Sparks T, Ventzek PLG, Smirnov VV, Stengach AV, et al. 2007. A molecular dynamics investigation of fluorocarbon based layer-by-layer etching of silicon and SiO_2. *J. Appl. Phys.* 101:033308. Copyright © 2007, American Institute of Physics.

A molecular dynamics simulation of layer-by-layer etching of Si and SiO_2 using fluorocarbon and Ar^+ ions has been reported; results of these calculations for Si etching at three different ion energies are shown in **Figure 13** (146).

ALE studies also indicate that fluorocarbon passivation layer thickness increases as CF_2^+ ion energy increases; F and C atoms also penetrate the underlying Si. Multiple exposures of Si or SiO_2 to sequential fluorocarbon and Ar^+ ions result in etching with nanometer-scale precision. Modeling results indicate that subnanometer fluorocarbon passivation films can be grown in a self-limiting manner on both Si and SiO_2 using low-energy (<50 eV) CF_2^+ and CF_3^+ ions. Increased ion energy yields thicker films, but eventually amorphization of the top atomic layers of the material occurs. Ar^+ etching of fluorocarbon-passivated Si also appears to be self-limiting at energies <30 eV, and etching terminates when surface F has been consumed.

Due to the inherently low etch rate of ALE, this etching method likely will be implemented for films thicker than ~30 nm only after a conventional etch has more rapidly etched the majority of the film so that a few monolayers remain. A simulation has been performed to investigate the feasibility of using conventional plasma equipment for ALE by utilizing a nonsinusoidal bias waveform to control ion energy and angular distribution (147). ALE selectivity and degree of surface roughening depended upon the ion energy of the etch step. In addition, control of both ion energy and cycle length is expected to play an important role depending upon the specific reaction mechanism. Although highly selective, the ALE recipes invoked in these calculations yielded effective etch rates of up to 4–5 monolayers $cycle^{-1}$.

ALE has also been applied to the etching of high-*k* materials. The use of ALE to fabricate HfO_2-gated n-type MOSFET devices demonstrated a 70% increase in drain current and lower leakage current compared with a device fabricated by conventional reactive ion etch (RIE) plasma etching. These results suggest that implementation of ALE techniques for nanometer-scale film etching can significantly decrease the structural and electrical damage incurred during device fabrication (142). The ALE technique developed almost 30 years ago did not find significant use in the IC industry due to a low etch rate; however, as the dimensions of the films involved in

device manufacture and their tolerance of defects and damage are scaled down dramatically, this method may develop new life.

SUMMARY AND FUTURE NEEDS

As is evident from the above discussion, surface reactions play a critical role in essentially every step employed in IC device fabrication. Although some of the manufacturing steps have not changed for 40 years, the mechanisms and kinetics of surface reactions that control film deposition, etching, and cleaning are still undefined. Considerably more fundamental understanding of these reactions will be needed to develop the processes and supply the control necessary for fabrication of ICs with minimum feature sizes of less than 35 nm. For example, despite the large number of studies of the cleaning/modification of surfaces using liquid and vapor (e.g., plasma, chelation) approaches, the active species responsible for etching/cleaning and the detailed reaction kinetics are undefined. In part, the lack of understanding is related to the complicated solution chemistries and to the complex and synergistic physics and chemistry of plasma-surface interactions; both need to be understood to achieve adequate etch selectivities for future device generations.

Plasma complexity also hinders establishment of the surface reactions involved in plasma etch processes, especially because intentional residue formation is currently invoked to generate anisotropic etch profiles and selectivity. In particular, the current use of polymers (as masking or passivation layers) produces additional challenges such as introduction of contaminants that must be removed to ensure high yield and high device performance. If novel processes based on chemical reaction selectivity can be developed to allow anisotropic etching and selectivity without the need for polymer or other residues, enhanced control of etch processes consistent with the demand for thinner films, smaller features, and shallower junctions could be achieved. Realization of these demands will likely require layer-by-layer techniques.

Because ALD or some related deposition method is required for future device generations to control the chemical, physical, and electrical properties of nanometer-scale films, a fundamental understanding of the surface reactions and interface interactions that control film deposition rates, chemical bonding structures, film stress, and film densities will be needed. Again, layer-by-layer approaches will likely be required because at these dimensions, excellent film conformality over existing geometries and precise thickness control at low growth temperatures must be achieved. In addition, if well-controlled selective deposition processes can be developed, photoresist/patterning processes could be eliminated, thereby simplifying the IC fabrication sequence and obviating the need to remove residues. Such deposition processes demand control of interface reactions and interactions because many film layers will be present during processing sequences, and interfaces generally affect and often control device properties and operation. Because ALD and selective deposition depend specifically on surface reactions, individual processes likely will need to be designed for each film material used.

To achieve successful device and IC fabrication, the numerous steps required must be integrated into a manufacturable process. This integration is crucial because surfaces and interfaces exposed to subsequent process steps can be altered and thereby modify device and circuit properties. The need for further understanding of the chemical reactions taking place at surfaces and interfaces has never been greater; the future of the IC industry will depend upon our ability to control these reactions at the atomic scale.

DISCLOSURE STATEMENT

The authors are not aware of any affiliations, memberships, funding, or financial holdings that might be perceived as affecting the objectivity of this review.

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